June 8, 1956

MODERN LARGE-SCALE COMPUTER SYSTEM DESIGN*

by

Walter F. Bauer

The Ramo-Wooldridge Corporation
Los Angeles, California

The objective of this report is to provide a survey of modern computer system design technology especially as it pertains to the use of large-scale systems for commercial and scientific purposes. The areas to be discussed are: Memory Devices, Information Storage and Internal Checking, Operating Speeds, Instruction Logic, and Input-Output and Off-Line Equipment. The components or design aspects of a number of modern computer systems will be referred to including the IBM-701, IBM-704, IBM-705, NORC, BIZMAC, UNIVAC I, UNIVAC II, Univac Scientific Models 1103 and 1103A, and the LARC. These are the computers available for rent or purchase, or built by organizations which rent or sell computers. Occasionally other computers will be referred to. Under System Design, the Project ERMA machine and the Office of Air Controller machine will be briefly discussed. In this survey and comparison, emphasis will be placed on the unusual or especially commendable aspects of the system.

Conspicuous by its absence here is a Bibliography of articles on the various machines and techniques presented. In this most rapidly changing field, most new developments are almost never found in books, and are seldom found in journals. The information recorded here was gained through reading manufacturers' reports and brochures, through discussions with manufacturers' agents, and through conversations with computer people generally. Manufacturers' reports, brochures, and discussions are available for the asking.

Memory Devices

The first operating stored program computer, the SEAC computer of the National Bureau of Standards, was equipped with mercury delay line memory. A short time later the ERA-1101 computer appeared with its magnetic drum memory. Again within approximately one year's time, the first cathode ray tube storage machines appeared, the first one of which, and most notable, was the Whirlwind I computer at M.I.T. The family of Institute for Advanced Study machines involved the Williams tube-type storage which was somewhat different in design from that of the M.I.T. storage tube design. More recently the trend is toward the magnetic core memory. The first machines of commercial availability which were produced with magnetic core memories were the Univac Scientific, Model 1103 computers, and the first one delivered went to the Operations Research Office of Johns Hopkins University in July, 1954. All succeeding 1103 type computers and the 1103A types to follow have magnetic core memories. With the more modern computers, again commercially available, the IBM-702 had electrostatic storage as did the 701. The 704 and 705 are equipped with magnetic core memories. The UNIVAC I is the only computer ever produced commercially with a mercury delay line type memory. Its successor, the UNIVAC II, to become available this year will involve a magnetic core memory for the basic high-speed internal storage device.

---

*This report arises from lectures the author has given in the special summer sessions on computers given at the University of Michigan in 1954, 1955 and 1956.

Thus the significant trend in memory devices is toward magnetic core memory. Early electrostatic memories were of rather low reliability. They required frequent adjustments during normal operating periods, and frequently the machine designers found it desirable to re-design deflection circuitries and other associated equipment. The result was that after two or three years of improvement gained through trial, error, and bitter experience, electrostatic storage became a reliable instrument and computers using this memory were very frequently recording reliability figures higher than 90%. However, the potential reliability of the magnetic core type is considerably greater. In private correspondence with William Papian of M.I.T., this writer received the following information in regards memory reliability of Whirlwind I after the replacement of the electrostatic memory with the core: "The main interval between memory parity alarms increased from a few hours to about two weeks, while the maximum interval went up from a few days to approximately six weeks. Specific memory maintenance time was reduced from a large figure to a couple hours per month". Thus, the reliability measured in terms of intervals between parity alarms or as represented by maintenance time increased by a factor of at least 10 in this case. Since probably upwards of 70% of the down time caused by electronic component failure (not including electro-mechanical devices) of a computer can be attributed to memory device failures, overall computer reliability will jump considerably.

Besides the advantages over electrostatic and mercury delay line type memories in areas of reliability, magnetic cores offer a tremendous speed advantage. The average access time with the mercury delay lines in the SEAC computer is 192 microseconds. This can be compared with the 6-10 microseconds access time with the core memories. Magnetic cores offer only a slight margin of greater speed over electrostatic types since electrostatic memories usually operate in the 10 or 12 microsecond region (some considerably higher), whereas magnetic cores operate in the 6-8 microsecond region. Specifications and characteristics of a number of modern computers are given in Table 1. The 4 microsecond memory cycle of the LARC computer as presented there is essentially an effective cycle since the design is such that there is a 2 microsecond overlap between the next operation and the last 2 microseconds of the normal 6 microsecond cycle time of the memory -- that is, the normal memory cycle involves something like the following: 2 microseconds for select and 2 microseconds for the destructive read. Selection of the next read is performed simultaneously with re-writing the information destructed in the reading operation.

It is generally agreed among computer designers that the conventional ferrite core cannot be switched at speeds which would result in basic cycles considerably less than 4 microseconds. Certain investigations continue in the direction of non-destructive read techniques. Also, it is expected that the future will show shorter memory accesses with a magnetic device called the "film wafer". In this technique, the resulting magnetic field is extremely low in power and consequently can be switched at extremely high rates. Signal amplification and reliability will be the critical obstacles in this development.

Memory sizes are increasing as fast as memory speeds. The conventional high-speed computer for scientific purposes has 4,096 words of magnetic core storage with options of 8,000 and 12,000 words, and in some cases an optional 32,000 word core memory. Table 1 lists the memory sizes available, together with certain optional sizes. High capacity, ultra-high access memories are necessary in scientific computing activities. Most large-scale scientific installations are happy with 4 to 8,000 words of high-speed storage. The IBM

Computer	Memory Type	High Speed Storage* Access Time	High Speed Storage Capacity	Drum Memory
IBM-701	Cathode Ray Tube or Magnetic Core	12	2,048 or 4,096	8192 words
IBM-704	Magnetic Core	12	4,096, 8,192 or 32,768 words	8192 or 16,384 words
IBM-702	Cathode Ray Tube	23	10,000 characters	60,000 characters
IBM-705	Magnetic Core	17	20,000 characters	60,000 characters
NORC	Cathode Ray Tube	8	3,600 words	- - -
BIZMAC	Magnetic Core	20	4,096 characters	16,368 or 32,736 characters
UNIVAC I	Mercury Delay Line	400 (max.)	1,000 words	- - -
UNIVAC II	Magnetic Core	40	2,000-10,000 words	- - -
Univac Scientific Model 1103	Cathode Ray Tube or Magnetic Core	12 8	1,024 words	16,384 words
Univac Scientific Model 1103A	Magnetic Core	8	4,096, 8,192 or 12,288 words	16,384 words
LARC	Magnetic Core	4	20,000-97,500 words	3,000,000 words

*in microseconds

COMPUTER STORAGE

TABLE 1

Corporation has announced the future availability of a 32,000 word magnetic core storage. The three options available are 4,000, 8,000, and 32,000 words with respective monthly rental figures of approximately $6,000.00, $12,000.00 and $15,000.00. The difference in rental price between 8,000 words of core storage and 16,000 words of drum storage, as compared with 32,000 words core storage, is almost negligible. Because of this, most installations who have need for 8,000 words of magnetic core and a considerable amount of drum storage are ordering the 32,000 word core storage. Presently, up to 12,000 words of magnetic core storage are available on the 1103A computer, together with 16,000 words of drum storage. It is expected that optional replacement of the magnetic drum with magnetic core will be announced soon.

Dr. Edward Teller of the University of California Radiation Laboratory at Livermore which wrote the specifications for and ordered the LARC computer, opined at the Western Joint Computer Conference in San Francisco in January, 1956, that the 50-100,000 words of high-speed storage to which people have occasionally referred, does not appear on the horizon as a necessity for the hydrodynamics applications of that group. Essentially, the Livermore group feels that the 20,000 words of core storage will suffice. The interest in the 32,000 words of core storage in connection with the IBM computers as referred to above largely results only from the fact that the small increase in price is attractive even in view of the increase, only moderate, in flexibility and convenience with the capacious high-speed storage. There is little doubt, however, that the future will see many problems requiring 32,000 word, or larger, core memories.

The need for a moderate-speed, medium access and high volume storage for commercial purposes is great, however. IBM has recently announced the IBM-305 Magnetic Disc memory. This memory will allow relatively low access to 5 million characters of information stored on discs to which reading and recording heads will travel for read and write operations. Remington Rand had included in their LARC proposal a magnetic disc file which would allow access to each of two million words of information in less than one second. This has been removed from the LARC equipment complement but a reasonable guess is that equipment of this type is contemplated for future systems.

On Table 1 there is also included the drum storage available on the various computers. The drums on the 701, 704, and 705 computers turn at rates which give maximum access times of 100, 25, and 16 milliseconds respectively. The drum on the Univac Scientific models turns at about 1800 r.p.m. with a consequent maximum access time of 35 milliseconds. The addressing scheme on the Univac Scientific drums is such that each of the 16,384 words can be addressed directly and can be used as an operand in the instructions. There is a trend in magnetic drum storage devices toward a higher pulse density with more modern techniques such as non-return-to-zero recording. This results in greater storage capacity for a given size drum and a higher transfer rate after the waiting or access time. It is of small consequence to the user except for the fact that it will probably result in a lower cost per item stored on magnetic drum. All of the magnetic drums on these computers are of the "single head type" -- that is, one head is used for both reading and writing on each track. It is also interesting to note that since these drums are used for semi-bulk storage, no schemes for reducing access time such as the circulating registers on the ElectroData computer and the Bendix G-15 computer are in evidence.

Computer	Tape Checking	Magnetic Tape Type	Transfer Rate
IBM-701 Model 1	Parity bit	Type 726*	1250 words/second
IBM-701 Model 2			2500 words/second
IBM-702	Vertical and		15,000 char/second
IBM-704	Horizontal	Type 727	2500 words/second
IBM-705	Parity bit		15,000 char/second
NORC	Bit count-modulo four Digit count Illegal Combinations	Modified Type 727	4,000 words/second
BIZMAC	Parity bit	Special	10,000 char/second
UNIVAC I	Parity bit, character count, and automatic re-read	Uniservo I	12,800 char/second
UNIVAC II	Parity bit, character count, and automatic re-read	Uniservo II	20,000 char/second
Univac Scientific Model 1103	Double recording	Raytheon	200 words/second
Univac Scientific Model 1103A	Parity bit and character count	Uniservo II*	3,300 words/second
LARC	Parity bit, character count, and automatic re-read	Uniservo II	2,000 words/second

*first models equipped with Uniservo I with parity bit and character count checks

MAGNETIC TAPE UNITS

TABLE 2

On Table 2 there is recorded the major characteristics of the various tape units used with the large-scale computers. It is interesting to note that all of the tapes involve the parity bit for checking. Also, all of these tape units record the information as 6 bits plus a parity check bit plus a bit serving as a timing channel. The horizontal parity bit on the IBM 727 tape units is an innovation and involves forming parity bits for each of the 6 information channels of the entire unit record after each record is recorded. In the case of a parity bit failure with the Uniservo I and II equipments, the information is re-read automatically twice with bias voltages changed, and the parity bit re-checked each time. The Uniservo I equipment to be used with the first models of the 1103A involves, in addition to the parity check bit, the placing of a certain code word in a register upon the occurrence of a parity bit failure. By means of programming, the information can be re-read with high and low bias voltages with the expectation that such re-reading will be performed correctly.

The obvious trend with magnetic tapes is toward an increase in speed and recording density. For example, the transfer rate of the tapes used on the 1103A will be ten times greater than the Raytheon units used with the 1103, and at a later date the Uniservo II equipments will provide an increase factor of about 16 over the Raytheon units. The very high transfer rate on the special magnetic tapes of the NORC computer is achieved primarily by the high recording density of 510 pulses per inch, and 140 inches per second.

It is interesting to note that none of these computers have the means to accomplish independent tape search. We refer to the ability to command a search for a particular block of information on magnetic tape and have the search carried out while computation proceeds. This feature is found on many of the smaller drum computers. While simultaneous read and write is possible with both the Univac and IBM-705, it is interesting to note that complete flexibility such as simultaneous writing on two or more tape units is still an item for the future in large-scale system design.

Information Storage and Internal Checking

There exists a definite trend in large-scale computer system design toward the handling of numerical information in decimal form and the ability to handle the full keyboard of alphabetic characters. The scientific computers now on the market still use the binary type of internal storage; however, it is likely that the 704 and the 1103A will be the last scientific computers to use the internal binary number system. This will probably be true despite the feelings of certain groups using scientific calculators that the storage of numerical information in binary form has distinct advantages in performing the complicated programming logic desired in scientific applications. It is entirely possible that future scientific computers will include the logic to handle both decimal and binary information.

The internal checks mentioned in Table 3 involve that checking performed in the machine in the control unit and in transfers between the various units such as transfers between the memory unit and control unit. We have discussed checking features above in connection with magnetic tape units.

Perhaps the situation in regards internal checking which is most in evidence is that internal checking features are increasing in number.

Computer	Word or Character Length	Storage Item Type	Internal Checking
IBM-701,704	36 binary digits/word	Binary	- - -
IBM-702,705	6 binary digits/char.	Decimal-Alphabetic	Instruction verification, Parity on transfer
NORC	16 decimal digits and sign/word	Decimal	Bit count and arithmetic check
UNIVAC I, II	11 characters and sign (or character)/word	Decimal-Alphabetic	Parity on transfer, arithmetic check
BIZMAC	6 binary digits/char.	Decimal-Alphabetic	Instruction verification Parity on Transfer Parallel arithmetic and control
Univac Scientific Model 1103, 1103A	36 binary digits/word	Binary	- - -
LARC	11 decimal digits and sign/word	Decimal	Parity on transfer Illegal combination check

INFORMATION STORAGE

TABLE 3

One notices that the 701 and 1103 had no internal checking at all. The trend is seen especially in the computers for business. This is probably due to the fact that one number wrong out of a thousand numbers is not catastrophic in scientific work; usually the scientist knows on the basis of reasonableness what to expect and can ferret out the incorrect value from many. Also, many scientific problems allow a natural check. For example, the answer to a linear system of algebraic equations can be checked by re-substitution thereby allowing, in a few seconds, a complete check on hours of computer time. In the case of the business application, however, one wrong answer often means an irate employee or customer (or ex-customer). Another factor may be the rather conservative outlook which the businessman has toward electronic devices.

The design of Univac I centered around the requirements of the Bureau of Census, for the first Univac was delivered there in 1951. The Bureau specifications called for a machine having ample checking features for the assurance of the correct processing of the large amount of census data. In the Univac this was accomplished by building parallel arithmetic units and control units which perform the operations twice, simultaneously and independently, followed by an appropriate check. The trend is away from such parallel construction which implies duplicate equipment and toward other types such as parity checks on transfer. Despite certain shortcomings evident today, it is truly amazing that the Univac, designed 7-8 years ago, has withstood the test of time in the face of extremely rapid technological improvements.

Some of the more common checks in use today are as follows:

1. Parallel arithmetic
2. Parity bit on transfer
3. Illegitimate combination
4. Arithmetic checks
5. Instruction verification.

The parallel arithmetic check of the Univac has been described above. Parity bit check on transfer is perhaps most commonly used today. On each transfer between the various units the parity bit is checked and the machine halted or a signal initiated upon the detection of an improper parity. The illegitimate combination check implies that a check is made to see whether the character code is legitimate or whether the instruction code is in the computer repertoire. With the character code check for computers performing decimal arithmetic the four binary digits (or, in some cases six binary digits) representing one of the digits from 0 to 9 would be checked to see if the combinations 10 through 15 were present. This type of check is very popular in medium-speed computer design and is included, as examples, in the Datatron and IBM-650.

The arithmetic check usually involves the carrying of a check digit along with operands in the arithmetic operations. These check digits remain invariant under the operation. As a result of the same operation performed on the check digit a check can be made to determine whether that digit is appropriate to the result. This type check is found on the NORC computer. The bit count check of the NORC is essentially a parity bit but sums the binary digits modulo 4 rather than modulo 2 as with the parity bit.

The instruction verification check is found on the IBM-702 and IBM-705 computers and involves checking an instruction while it is being performed to

determine whether the instruction code digits are legal and have been interpreted correctly.

Operating Speeds

In Table 4 there is shown the operation times for the computers. All operation times include the appropriate number of accesses to the memory including the access time necessary to get the instruction itself. This implies 2 accesses for the 704, 3 accesses with the 1103, and 4 with the NORC. Arithmetic operation times on the 702, 705, and the BIZMAC, those computers intended solely for business applications, are based on the assumption that all operands are 5 digits in length.

No important trends are in evidence here except the obvious one that computing times for the scientific computers is drastically reduced with the announcement of each new system. The most recently announced computer, the LARC, has the remarkable addition time of 4 microseconds, achieved mainly by an overlap between instruction execution and memory access. Recently, the University of California Radiation Laboratory at Los Alamos asked for bids on a computer which would have an addition time less than one microsecond including memory access. The response to this request will probably be a proposal representing a computer considerably more advanced than the LARC.

There are a number of interesting comparisons. For scientific computations the 704 enjoys a wide margin of speed over its predecessor the 701 besides the floating point feature which the 701 does not have. Since the 1103A is almost completely program-compatible with the 1103 the differences in time reflect only the difference in operating speeds between the electrostatic and the magnetic core memories. The add and divide times for the 1103 (1103A) are seen to be considerably slower than those of the 704 while the multiply times are comparable. The NORC will most likely be the fastest computer in operation until early 1958 when the LARC appears.

Operating speeds for the commercial computers are considerably less important. The core memory of the 705 has given it a considerable speed advantage over the 702. The greatly increased speed of the Univac II over its predecessor Univac I will no doubt allow greater convenience and flexibility in those commercial applications where computation must proceed simultaneously with tape transfers as it does in most cases.

Instruction Logic

A short time ago a divergence of opinion close to a controversy existed between the advocates of the single address logic and advocates of the multiple (usually three, cometimes four) address logic. In 1951 the SEAC and Mark III computers with their four- and three-address logic were compared with the Whirlwind and ERA-1101 with their single address logic. Champions of the single address got a big boost when the so-called Princeton (Institute for Advanced Study, or von Neumann) machines and the IBM machines appeared. Except for the NORC and the 1103 and 1103A, all the large-scale computers of Table 5 have single address instruction structure, thus indicating the rather general acceptance of the advantages of single-address logic.

Computer	Addition Speed (in microseconds) Fixed	Addition Speed (in microseconds) Floating	Multiplication Speed (in microseconds) Fixed	Multiplication Speed (in microseconds) Floating	Division (in microseconds) Fixed	Division (in microseconds) Floating
IBM-701	60	--	456	--	456	--
IBM-702***	253	--	1058	--	2380	--
IBM-704	24	84	240	204	240	216
IBM-705***	119	--	799	--	1819	--
NORC	56	56	72	72	272	272
BIZMAC	420	--	2324	--	--	--
UNIVAC I	520	--	2200	--	4000	--
UNIVAC II	200	--	1880	--	3680	--
Univac Scientific Model 1103	55	--	276	--	500	--
Univac Scientific Model 1103A	42	181	270	262	490	664
LARC	4	4	12	12	60	60

All times include memory accesses for instruction and operands.

***Assumes 5-digit operands

OPERATING SPEEDS

TABLE 4

Advocates of the single-address logic say that it is natural that the programming processes are similar to those of a desk calculator, the accumulator of the high-speed device having the central dials as its counterpart on the mechanical device. Despite the advantages, certain important disadvantages exist in a hypothetical system where there is an accumulator and one can use instructions, each with a single address. Take, as a simple example, evaluating the algebraic expression ab+cd. After multiplying a by b the result must be removed from the accumulator so that the product cd can be formed there. Later ab is essentially returned to the accumulator for formation of the final value. As another example, suppose in the commercial application a part number is being searched for. The part number is stored in the accumulator and is compared with, say, part numbers from magnetic tape. As each part number is compared with the one sought, the number is removed from the accumulator so that it can be used for address modification. In each of these cases it seems desirable to have a second accumulator and an instruction logic which can make use of either one. In each of the examples cited approximately one out of six instructions could be saved by the second accumulator.

Advocates of multiple addressing schemes point to the flexibility and convenience in using two and three address instructions in logical and transfer of control operations. Consider the conditional transfer of control operation. Advocates of the two address logic, for example, would point out that the two branches of the program are clearly and explicitly given in the instruction; the contents of address X is compared with the accumulator and control either reverts to the next instruction or to Y, the other address given. These people would say that this is handled awkwardly in the single address scheme where two instructions are necessary to handle the normal program biforcation: one to form the difference between the quantity in X and the accumulator, another to transfer if that difference is positive.

Nevertheless, the single-address instruction logic, in overall evaluation probably scores highest, for, besides advantages to the user, it offers certain simplicity in the control components. However, the addressing system apparently gaining popularity may be referred to as the "augmented single address" or the "one-and-one-half address logic". In this logic there is only one address, and, therefore, only one operand involved in operations with the accumulator. However, the accumulator has a number of parts or a number of special registers are available for use with certain orders. The normal operations are modified (or subdivided) into similar operations but dealing with a special part of the accumulator or a special register. Although none of the large-scale systems have progressed far along these lines, the IBM-705 does indeed have a total of 16 accumulator registers, each one of which is available for addition and comparison operations.

The idea of having certain special registers is certainly not new. Most single address computers have an "x register" or something equivalent. However, there will no doubt be an increasing use of these registers for greater flexibility and more powerful operations.

The "polynomial multiply" instruction is an example. This rather new instruction takes the contents of the accumulator, multiplies it by the contents of address A, adds the product to contents of B, leaving the result in the accumulator. One sees that with this process one makes one step in evaluating the polynomial in the "inside out" manner as indicated by

$$\left\{ \cdots \left[(A_n X + A_{n-1}) X + A_{n-2} \right] X \cdots \right\} + A_0$$

This operation is performed very frequently in scientific computation. The Univac Scientific Model 1103A will be equipped with this instruction. No special X register is necessary with the 1103A since it has a two-address scheme. However, the future will no doubt see more of these special registers with their attendant flexibility. As a matter of fact, the LARC will have two decimal digits of the instruction word reserved to specify (up to 100) special arithmetic registers. IBM will soon announce changes in the 704 which will be along the lines of more powerful instructions such as the polynomial multiply mentioned above.

Let us examine Table 5 containing an evaluation of the instruction logic of six large-scale computers intended primarily for scientific applications, and Univac I and II, intended mostly for commercial applications but used to great extent in scientific work. Despite the fact that the 705 is not listed in the table, it should be realized that its variable word length operation means that it can be profitably used on many scientific problems, especially those involving extra-precision or programmed floating point.

"Address Modification" is the first category. A computer with the B-register for automatic address modification gets the "excellent" rating, all others the "fair" rating except the 1103 and 1103A which have the "repeat" feature which allows automatic address modification with less flexibility. The B-register is an important feature, since machines equipped with it probably use 15-20 percent less storage for instructions and operate about 10 percent faster on representative problems.

The next category, "overflow handling", involves the provisions for the detection and handling of overflow in arithmetic operations. The 701, 704, NORC, Univac I, and II all have the ability to interrogate by means of the program whether overflow has occurred and, therefore, the ability to correct it quickly and automatically by means of the program. Optionally, these computers will halt on overflow detection. The 1103 and 1103A have only an alarm which stops the computer on alarm detection. The LARC will have a complete detection system which will allow an automatic jump to one of a number of registers depending on the operation producing the overflow. Overflow handling with the floating point computers (704, NORC, 1103A) is not as important as with those having only fixed point operations.

"Program Checking" features are those designed to help the programmer in rapid programming mistake diagnosis. The 701, NORC, and 1103-1103A have virtually no built-in features for mistake diagnosis. The Univac I and II have breakpoints which allow the programmer to halt the computer (or cause change of control) at specified points in the program. The 704 has a "trapping mode" which allows high-speed tracing of the program by causing control jump to special cells and the wherewithal to return when the program reaches any jump instruction. The LARC will have an elaborate breakpoint system and will, in addition, allow the programmer to address the "current instruction counter" directly. Also, the address of the "last jump" will be filed and will be available directly to the programmer. This provides the wherewithal for the development of extremely high-speed, complete program "debugging" routines.

The "Arithmetic Operations" category refers to the part of the machine logic designed to make arithmetic easy and convenient. Taken into account here are instructions for double precision, floating point (by programming), and ease of accomplishment of arithmetic operations. It is

Computer	Address Modification	Overflow Handling	Program Checking	Arithmetic Operations	Logical
IBM-701	Fair	Good	Fair	Good	Fair
IBM-704	Excellent	Good	Good	Good	Good
NORC	Excellent	Good	Fair	Good	Good
UNIVAC I, II*	Fair	Good	Good	Fair	Fair
UNIVAC Scientific 1103, 1103A	Good	Fair	Fair	Good	Excellent
LARC	Excellent	Excellent	Excellent	Excellent	Excellent

*The UNIVAC is included here although not primarily a machine for scientific calculation.

INSTRUCTION LOGIC EVALUATION

TABLE 5

comparatively somewhat awkward on the Univac I-II to perform addition since three instructions (one and one-half words) are necessary. Also the Univac I-II does not have a double length accumulator convenient in arithmetic operations. The 1103-1103A has the multiply-add instruction which allows, in one instruction, a multiplication and an addition of the product to a previously obtained quantity, and provides, with the use of the repeat instruction, evaluation of a vector inner product $(a_1b_1+a_2b_2+\ldots+a_nb_n)$ with only two instructions. As previously mentioned, the 1103A will be equipped with a polynomial multiply instruction in floating point. The most recently designed computer, the LARC, will have a host of instructions for convenient arithmetic operations. Included, for example, are instructions which will actually perform double precision arithmetic operations.

The column of Table 5 headed "Logical" refers to all aspects of the instruction logic which are non-mathematical and are not specifically mentioned in the remaining columns. Included here are all those instructions which reduce the programmer's "red-tape" such as subroutine handling, extraction of parts of the computer word, etc. The IBM-704 has the "logical and" and "logical or" commands which are powerful and flexible. The 701 does not have the ability to "file the current instruction register" to make subroutine handling smoother. The 704 does have this feature which is used in conjunction with the index registers.

The 1103-1103A, with its two address logic, has a complete set of jump instructions which are easy to use. One of these is a "Q-jump" which examines the left-most bit of the quotient register and jumps control or does not jump, depending on the presence of a binary 0 or 1, and then shifts left one binary digit. This allows the storage of a complete jump sequence in readily available form. The 1103-1103A also has the "interpret instruction" which jumps control to a specific cell and files the instruction counter, thereby allowing 30 digits to the program to specify any interpreting language he wishes handled by subroutines. The 1103A has an "interrupt feature" by means of which an external equipment operating asynchronous to the computer can interrupt the program and cause transfer of control to a specific cell with the instruction counter filed for later access. This allows programming convenience in input-output operations, and also allows application to devices such as analog-digital conversion devices. The LARC has a complete complement of instructions of this type. A rather unusual instruction is one which performs a "logical inclusion" test, thereby checking whether the binary ones in a word are included in the binary ones of another.

A discussion of future trends in instruction logic turns to the LARC. This machine will have addressable error registers for overflow of various causes, arithmetic error, and transfer error. Presumably bits will be introduced into these registers for program interrogation and subsequent automatic program handling. Also, all B-registers will be directly addressable as well as the current instruction counter and the counter at performance of the last jump instruction. The addressability of all these counters will be of great convenience to the programmer and will no doubt be generally found in all future large-scale system design.

There are two ways of handling overflow, arithmetic and transfer errors: 1) have bits introduced into certain cells (or flip-flops set) which are later interrogated, or 2) have control transferred to a cell upon occurrence of one of these conditions. The former way is the design of the

701, 704, and 705. It is not clear at this early date what the design of the LARC in this regard will be. It is the opinion of this writer that the second method is more desirable. Automatic transfer to the appropriate error register will allow uniform treatment of the condition by all programmers. Also, placing the appropriate command in the error register to handle possible errors will be similar to setting a manual switch by automatic programming means; it should be realized that putting a halt instruction in the register would correspond to putting the overflow switch (or other switch) in the halt position. As a last reason for the first method, it will reduce the amount of program instructions in cases where a uniform treatment of a given type of error is possible over a large portion of the program as is usually the case.

The interrupt feature of the 1103A will no doubt be embodied in many future computers. This feature, which allows program interruption by equipment operating asynchronous to the computer, will allow, for example, greatly simplified timing of the row-read instructions in card reading operations. Also, it will allow convenience in the use of analog-digital conversion devices, for with it a clock source outside the computer can tell the computer when a new quantity has been (is to be) sampled. As a matter of fact, future computers would do well to have perhaps as many as five interrupt channels so that interruption due to five different causes can be distinguished.

The overall trend in instruction logic is to provide an increase in programmer convenience and automatic machine operation to reduce idle time. These increases are at the expense of complexity of computer design and construction and will result in more expensive computers. An increase in programmer convenience is necessary for survival in this era of the national programmer shortage. The two most important additions for programmer convenience are the B-register and floating point. Others, mentioned above, will follow. The other item, the increase in automatic operation, is just as essential in this era of high-speed and high cost computer operation. The implicit cost of the non-productive computer time used while the machine operator reaches for a manual switch is appalling and will become even more so. In the future all large-scale machines of good design will have the ability to change all switches at high speed by program control. Future changes on the 704 will include this feature. Duty cycles of computers will be increased; it will not be unusual for computers to work on two problems simultaneously by means of an interrupt feature. Other inclusions will be available for increased automaticity. The Whirlwind I computer at M.I.T. already has the ability to interrogate a time clock under program control and has an "idling alarm" which, if not interrogated in the program at regular intervals sounds and informs the operator of the idling of the computer or its being caught in a tight program loop.

System Design

The system design of most computers available today for rent or purchase can be called conventional. This system design consists of a central data processing unit with copious numbers of input-output devices with which it communicates. This communication, as will be discussed in more detail further below, is implemented by the central processor having the ability, under program control, to start an external equipment in motion and to transfer information from its memory to a limited buffer storage device from which the information is taken by the external equipment. In this design the system performs only one operation at a time -- the operation in regards external or auxiliary equipment is serial. The important trend from this conventional

system is toward one with larger buffering storage and simultaneous operation of many auxiliary equipments. This trend is best illustrated by the system design of four computing or data processing systems: ERMA, the Electronic Recording Machine - Accounting; the RCA BIZMAC; the OAC Computer, Office of Air Controller; and the LARC. The OAC computer is designed to handle the large scheduling and logistics problems of the Air Force, and ERMA is a system designed at Stanford Research Institute for the Bank of America. The BIZMAC, the only one of the four in the hands of a user, and LARC have been referred to previously. The ERMA will be built by General Electric and will no doubt involve a construction (and sales) program beyond the 30-odd machines intended for the Bank of America. This writer does not know whether the OAC computer will be built.

Project ERMA was conceived to build a machine to handle the commercial account problem -- check handling and accounting -- for the Bank of America, probably America's largest bank. As illustrated by Figure 1, the system consists of an input device which reads check and deposit data into a magnetic drum

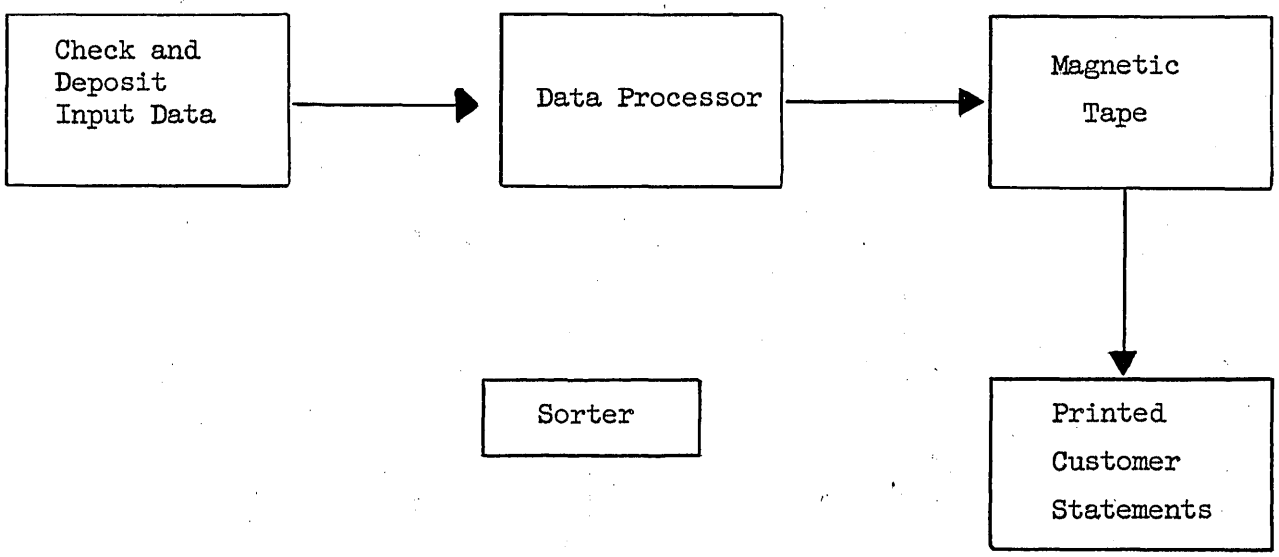

Figure 1

processor. Periodically, information from drum storage is read from the drum memory onto magnetic tapes for subsequent printing of customer statements. A sorter, completely apart from the rest of the system, sorts checks for return to the customer along with the statement.

With this system all checks and deposit slips will have a customer account number printed on them with a "magnetic ink". Customers use the standard forms or pay extra for the unusual handling of non-standard forms. Clerks working at 5-10 input stations input the dollar amounts of the checks or deposit slips by means of keyboards. The machine automatically reads the account number and the two pieces of information are recorded on a magnetic drum. Also recorded on the magnetic drum is the customer's balance and information on the "holding" or "stopping payment" of checks. If no hold or stop payment action takes place, the amount of the check (or deposit) is deducted (added) to the balance. Periodically and automatically, as the drum fills, information

is tapped off the drum, sorted by account numbers, edited and recorded on tape to provide the desired account statement to the customer.

The ERMA machine is strictly speaking not a computer but is rather a special purpose device much like the Speed Tally system for mail order house use or the Reservisor for airline seat reservation handling. The operators can exercise little control on the course of events, no programming is necessary or possible and, by and large, the machine performs the same operations day to day. However, it must be said that the very real problem of handling checking accounts is handled reasonably well by a system which allows a simultaneous input, data processing, and data output.

The system design of the BIZMAC is unusual or at least does not closely resemble the conventional computer system design. As indicated in Figure 2 the system can be thought of as five groups of components each using tape units of the magnetic Tape File. The computer is general purpose with magnetic core and magnetic drum internal memory, and can read and write

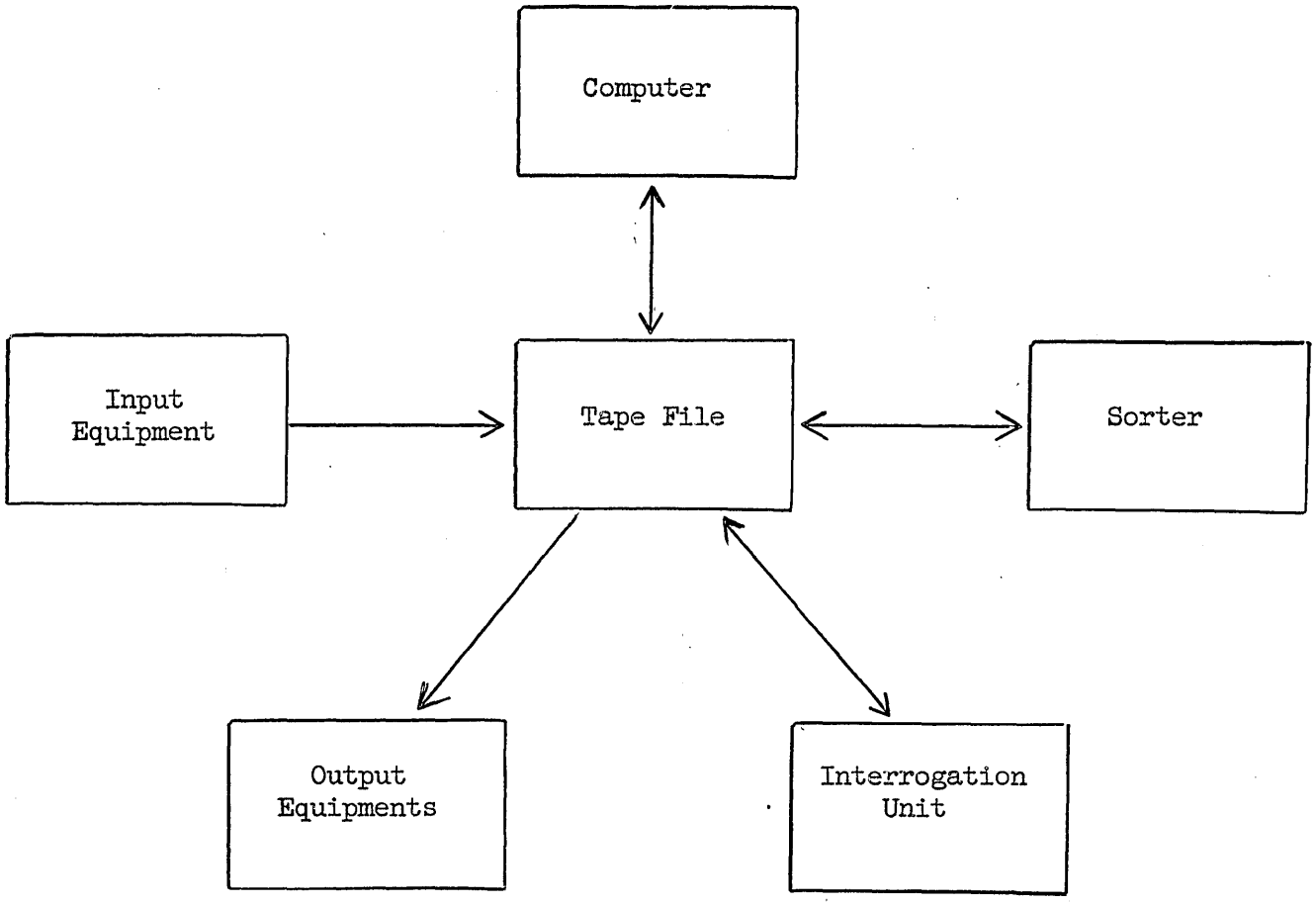

Figure 2

information onto the tape units. The sorter is a special purpose computer for arranging, merging, and extracting data stored in the tape file. The interrogation unit has facility for selecting a particular message from the tape file and printing it locally. The output equipments consist of a high-speed, 600 line/minute printer, high-speed camera allowing 4,000 character per second output,

and a paper tape punch. Each of these is magnetic tape-driven. The input equipments which input data to the tape file consist of a magnetic tape input, and an IBM card input. In addition to the input-output equipments described there is a keyboard machine to produce paper tape and a typewriter which is paper tape driven.

The important fact to realize about the BIZMAC system schematized in Figure 2 is that the whole system is not under the control of the computer. Each equipment communicates only with the Tape File. The Computer, Sorter, and Interrogation Unit control or use the Tape File, each in its own way: the Computer under program control, the Sorter and Interrogation Unit as a result of manual switch initiation. The various units are manually connected to the Tape File by means of a control console plugboard. Apparently only the computer can select tape units at high speeds and in complex logical situations. Once certain manual plug-ins have been effected the system does allow simultaneous operation of the many units. The Sorter, although it can work simultaneously with the computer, is of somewhat limited processing power, and the Interrogation Unit can only search for file items. The Input-Output Units operate to and from magnetic tapes like most equipment offered by Remington Rand and IBM.

The design of the OAC computer would allow it to handle the large matrix operations of Air Force program scheduling. Since that application is not fully or finally defined, the design is such as to allow expansion to a greater number of units or substitution of faster units for slower ones. Particular emphasis was placed on the input-output problem and the resultant scheme essentially uses the entire memory as input-output buffer storage.

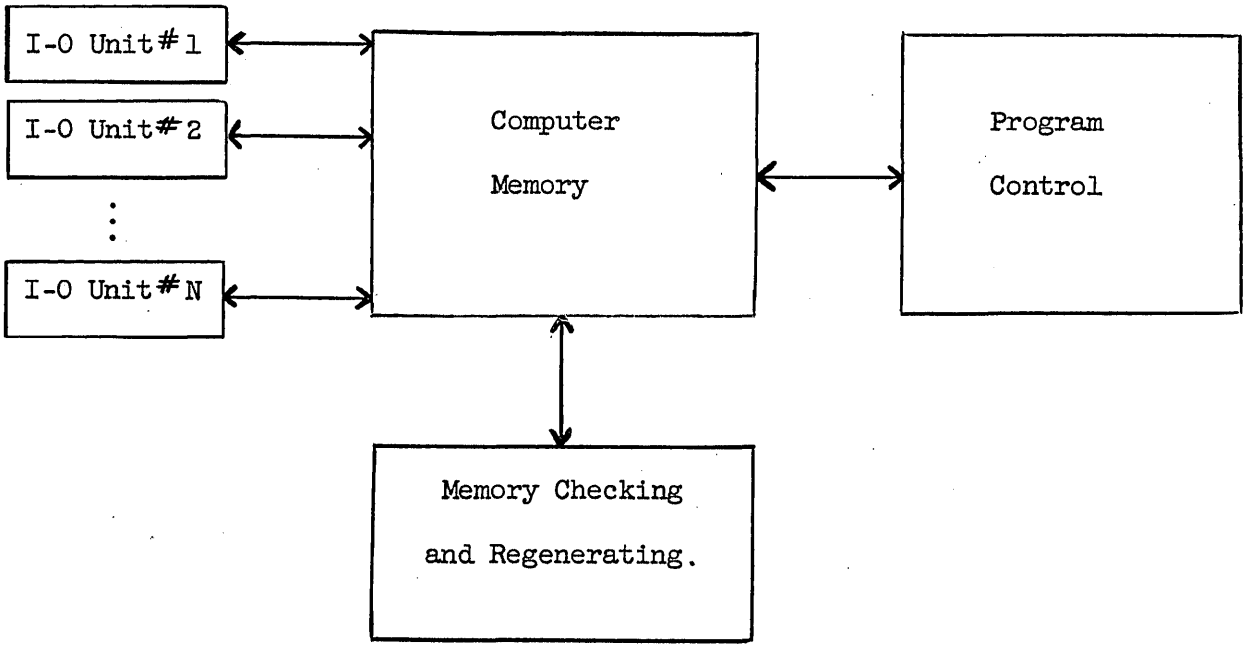

Figure 3

The system shown schematically in Figure 3 consists of a high-speed memory which communicates with three devices: the Program Control unit consisting of the arithmetic and control sections, the Memory Checking and Regeneration unit, and the Input-Output units. Under program control the computer will command transfers to input-output units from the memory. Transfers

can occur simultaneously with normal computation except for time-sharing a shift register. The time scheduling of all in-out operations will be handled independent of the central computer control so that these operations will not interrupt normal computing; an input-output instruction causes a transfer to be accomplished subsequently as computing continues. Accesses to the memory by the arithmetic and control units will proceed simultaneously (or will be dove-tailed) with the accesses for input-output operations. The plan also calls for a separate Memory Checking and Regenerating unit which will proceed simultaneously, with its necessary memory accesses, with the operation of the computing and input-output functions.

Clearly the system design of the OAC computer allows the possibility of conflicts in the interaction of the various components. The conflict of two units requiring a simultaneous access to the memory is avoided by assigning certain machine cycles to the various units similar to the "time slot" idea of the LARC described below or the buffering concept on the modified 704. Conflicts between input-output devices for the high-speed memory are also avoided by setting up a time schedule by which each device, in turn, has access to the memory. Certain conflicts are not unavoidable and will cause an interlock condition to be set up until the conflict no longer exists. For example, if a transfer into the memory is not completed before an access to the same part of the memory occurs, the computer automatically idles until the transfer is completed. One sees that with this system design the input-output can proceed almost completely simultaneously with computation since essentially the entire memory is used as an input-output buffer register.

The LARC represents the most ambitious design of any system yet made available for general public information. The accent here is on modular construction: units comprising the system will be self-sufficient even for air-conditioning and may be added to or deleted from the normal system complement. The heart of the system consists of a number of Computing Units and one Input-Output Processor tied to a common information bus which is in turn tied to a number of memory units. Two Computing Units, besides the Processor, and as many as 39 memory units, each with 2500 words of high-speed storage and complete selection circuitry, are possible.* Twenty-four drums (six million words) and forty Uniservo II tape units, a 600 line per minute printer, a 25,000 character per second Charactron Tube (see Input-Output Equipments below), can be integrated into the system under control of the Input-Output Processor. Reference is made to Figure 4 for a schematic of the system. The computer is controlled by a number of consoles.

The system design of the LARC carries the idea of simultaneous operation of major units much further than in any other system while still keeping the desirable features of flexibility and the qualities of a single integrated automatic system. The Computing Units (CU) and the Input-Output Processor (I-O P) are complete computers in themselves except for memory

---

*The LARC system as initially ordered by the Livermore Radiation Laboratory will consist of one Computing Unit, one Input-Output Processor, 8 Memory Units (20,000 Words), 12 magnetic drums (three million words storage), 4 Uniservo magnetic tapes, a 600 line per minute printer and a Charactron Tube.

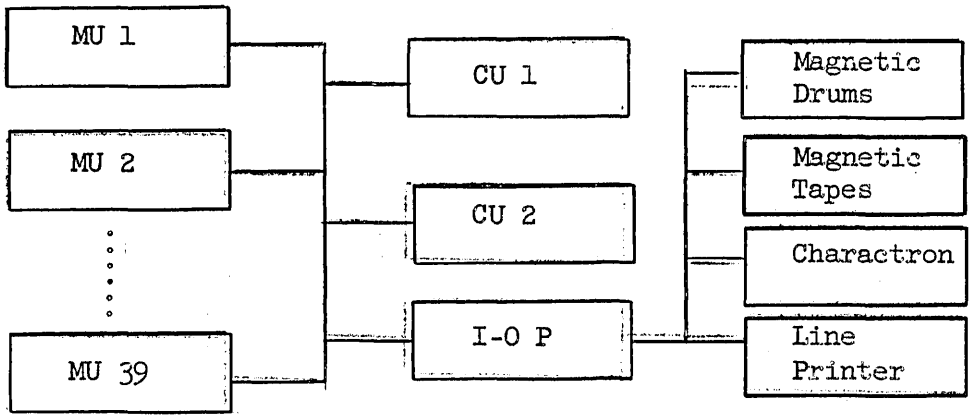

Figure 4

storage. The Processor will have a complete set of input-output instructions in addition to the arithmetic and logical ones but will be slower in operating speed than the CU's, its add operation requiring 16 microseconds. Each CU and the Processor will be able to operate on any quantity stored in the Memory Units (MU's). The CU's are designed for the basic computing function while the Processor is designed primarily to handle data transfers to and from the MU's.

It has been mentioned earlier that the LARC gains much of its computing speed by overlapping parts of successive operations in executing an instruction. This time-overlap is again seen in the use of the CU's and Processor in an interesting "time slot" technique for using the MU's. Since only one unit can use the information bus to the MU's, the four microsecond memory cycle is divided into eight one-half microsecond time slots, with each communicating unit assigned certain slots. The units then use the bus during the slots to address the memory. It will be possible, for example, for a CU to address Memory Unit 1 and 2 and the Processor address Unit 3 so that the three accesses are performed in only six microseconds, rather than approximately 15 microseconds without overlap.

In the full-blown LARC system it will be possible to use one or more CU's on one problem, along with the Processor, or to use the CU's on different problems each sharing the Processor. Communication between the units will be possible. For example, a CU will be able to signal a Processor that certain quantities have now been computed and require editing for output to tape units or transfer to drum storage. Most likely the system will operate as follows: upon the Processor's receipt of a signal from the CU it will examine a memory cell into which the CU has placed a code word to specify the input-output or transfer operation desired.

It is interesting to note that among these four large-scale processing systems chosen for their unique system design, two are intended for business purposes and two for scientific. Moreover, an important difference exists between the two pairs: the scientific computers largely operate as one large, integrated system in which all activities of input-output and processing are handled automatically in a pre-programmed sequence. In this sense the scientific computers are more conventional. However, all of these computers show the important trend of simultaneous operation of major components allowed by duplicating certain processing components and allowing intricate simultaneous use of a memory storage by the processor and input-output devices.

Perhaps it should be emphasized here that the discussion of the system aspects of ERMA and BIZMAC does not imply that these designs are endorsed over the IBM-705 or UNIVAC II. As a matter of fact, a comparison of these general purpose machines with the special purpose ERMA would be inappropriate. In connection with the remark made above concerning the trend toward simultaneous input-output and processing, it is pointed out that this trend was started by the 705 and UNIVAC systems with their off-line card (or keyboard) to magnetic tape devices and their magnetic tape-driven printers.

There seems to be little doubt that the automatic system concept has been carried much further in the case of the OAC computer and the LARC than with the ERMA or BIZMAC. Also, there seems to be little doubt that the large scale systems for business or science in use 5-10 years from now will more closely resemble the former pair than the latter. It seems certain that the completely automatic, pre-programmed machine will replace the manual, step-by-step operation. One easily imagines a LARC-type computer, for example, performing sorting with its Input-Output Processor simultaneously with central data processing with an occasional and automatic interrupt from central control to perform an input-output function. In the past five years the computer design and the design of the system around the computer has shown a strong trend toward saving expensive machine time. This has been evidenced on one hand by systems which allow computation to proceed during in-out cycles and on the other hand by allowing only professional operators (not programmers) to operate machines. This will become even more important in the future and the change from manual head-scratching-at-control-console to automatic operation throughout will become mandatory.

Another trend in system design which is just beginning is that toward "microprogramming". With this technique computers are designed to allow the programmer to construct his own computer instructions from "micro-instructions". A typical microinstruction might be "shift left one binary digit" or "round the number in the accumulator according to the 37th digit". Later, selection and composition of microprogrammed instruction will be done by plugboards or at electronic speeds under stored program control. To this writer's knowledge, only two university groups in the country have shown active interest: Servomechanisms Laboratory of M.I.T., and Numerical Analysis Research at University of California at Los Angeles.

The form for microprogramming in system design is not now clearly seen nor is the extent to which the techniques will be applied. The future may well depend on the speed with which microprogrammed instructions can operate. If every microinstruction requires many time-consuming memory accesses the operation speed will be slow and the technique unpopular. One recalls the fact that five years ago most computer users were content to perform floating point operations by interpretive programs even though the operating speeds were painfully slow. Later, the need became great to include floating point operations as hardware modifications. As soon as a microprogrammed instruction becomes popular, users will want to have it included as hardware unless it operates as fast as it would as a permanent hardware modification. Indeed, the computer of the future will probably have instruction repertoires 200-300 instructions in length and may have no need for a microprogramming facility.

Input-Output and Off-Line Equipments

Input-output equipment is here defined as that equipment used to get information into and out of the internal memory of the computer. Off-line equipments are those not directly connected to the computer and are usually means of transferring information from one external medium to another. Generally, the development of this electro-mechanical equipment has lagged behind the development of the computer proper. In the computer development of the last decade, it was difficult to forsee the need for a scientific computer to output words at the 2,000 word per second rates we have today and extensive commercial applications still seemed more than ten years away.

In 1951, before the magnetic wire system was developed, the SEAC computer, not a fast computer by today's standards, was badly out of balance; its paper tape read-and-punch input-output equipment required about 25 minutes to fill the entire 512-word memory. The use of punched card equipments with computer systems greatly helped the situation, especially when the IBM-701 was developed with its scheme for "dove-tailing" computing and input-output. More recently, magnetic tape devices have caused still further amelioration. Recently, cathode ray tube equipments have appeared which are even faster.

Besides speed, reliability has always been a problem. With most computing systems over half the down time is caused by input-output failures. As with speed, reliability has increased greatly during the years. Probably the greatest motivation for increased speed and reliability has been the use of computers for business applications. However, it is true that the increased complexity of computation systems for scientific applications has also increased the emphasis on input-output equipments. It is a most significant fact that the four firm orders (at this time) for the Univac Scientific 1103A systems include the Remington-Rand 600 line per minute printer.

In the early days of computers whenever an input-output function was called for, computation was interrupted while the asynchronous input-output equipment performed its operation. The Univac was the first computer to allow simultaneous computing and input-output (magnetic tape) operation. The IBM-701 computer first allowed simultaneous computing and input-output operations with a multiplicity of input-output devices. Thus the first input-output buffering systems were used.

In general, an input-output buffering storage system is designed for the purpose of allowing the computer to place information in the storage at computer speeds, leaving the information there for removal at the output equipment's rate, usually considerably slower. This does imply that a system of interlocks is necessary to allow for the possibility of poorly timed operations. Figure 5 illustrates an idealized buffering system, "single-stepped",

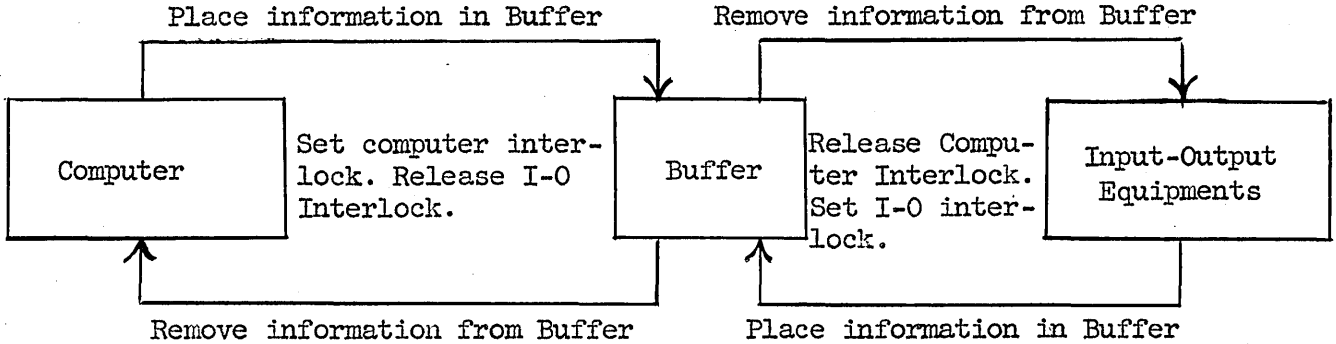

Figure 5

since the buffer only holds one item of information. When the Computer communicates with the Buffer, the computer is locked-out and the I-O interlock is released, allowing communication of the Buffer with the Input-Output. When communication of the I-O with the Buffer occurs the computer interlock is released and the I-O interlock set. In most cases the input-output equipment is "free-running" which implies that, during output, the output equipment continually and periodically samples the buffer. Information must be there or the interlock causes an alarm. By the same token, if the computer attempts to deposit a number in the Buffer and the computer interlock is not released, the computer will idle until the release occurs. Similar statements can be made about input.

The input-output buffering system of the 1103A is similar to the one described above. Two buffer registers are available. To choose an input-output device a code word is placed in the buffer. This starts the device in motion. Transfers then occur as described above. The system has the advantage that practically any kind of device can be attached to the buffer. Also two or more devices can be operated simultaneously. IBM will soon announce improved buffering with the 704. Under the new system two one-word buffers will allow tape transfers to proceed with minimum program control, and almost completely independent of normal computing. This much-needed change has not been announced thus far for the 1103A.

Clearly the larger such a Buffer storage is, the more useful it is. The 80 character buffer storage for card input-output on the IBM-705 allows much more economical operation than in the 701 where half-card rows were the maximum used. IBM's Tape Record Coordinator, Type 777, is essentially a 1024-character buffer which allows more convenient tape transfers. The 60-word input and output buffers of the Univac, the first computer to have extensive buffering, are still among the largest buffers available today.

A buffering system much more flexible than the system described above, is one where the buffer storage has a capacity of more than one computer word, or, better than this, the buffer stores any number of words up to some large number. In this system, the item drawn out by the input-output device is the one which has been in the buffer longest. Telemeter Magnetics, an affiliate of International Telemeter in Los Angeles, actually makes a magnetic core buffer register of such a design.

Input-output buffering takes an important step forward in the system design of the OAC computer and the LARC. With both of these computers, essentially the entire memory is buffer storage. Thus, almost completely independent operation between the computer and the input-output units is effected, with only the time-sharing of a high-speed information bus or shift register involved.

Punched paper tape has been used extensively as a computer information medium. Earlier Teletype readers and punches operated at about four characters per second. More recently the Flexowriter has come into favor because of its higher speed (8-10 characters per second) for reading and punching. For higher speed input, Ferranti, Limited, of England has made a photo-electric paper tape reader which reads at 200 characters per second and, utilizing a well-engineered clutch device, can "stop on a character". The "Ferranti Reader" is in extensive use in this country and in England. The Teletype Company makes a 25-character per second punch as well as a 60-character per second punch. Of all the large scale systems mentioned here, only the 1103A uses paper tape as an input-output medium (in addition to punched cards). Flexowriters are used off-line to punch and read tape. On-line a 60 character per second punch and Ferranti Reader are used.

Punched cards are, of course, infinitely more popular than punched paper tape. The universal use of the punched card in business accounts for much of this popularity. Paper tape users who try punched cards find them much more convenient, for they are easily stacked and placed in a neat form for handling which is certainly not the case for paper tape which requires awkward, inconvenient, manual handling. International Business Machines makes all of the punched card equipment used with computers in this country except for the Bull equipment on the 1103.** The Bull Company of France makes an 80-column, 12-row card reproducer which is licensed for use in this country by Remington Rand Univac. With this equipment, cards are read and punched under computer control at 120 cards per minute. With Bull equipment, a serious (for scientific uses) limitation exists: approximately only 140 holes can be punched in any card which implies that the card cannot safely be used to receive a full card's worth of binary information from the computer.

As a natural consequence of its accounting machine business, IBM makes a full range of punched card readers and punches. The Type 711 Model 1 card reader operates at 150 cards per minute and is used with the 701 computer. The Type 711 Model 2 reader, used with the 704, operates at 250 cards per minute. The Type 712 operates at 250 cards per minute and is used with the 702. The Type 714 is approximately the same as the 712 but has a control panel available which the 712 does not and is used with the 705. The Type 721 card punch operates at 100 cards per minute as does the Type 722, a later version used on the 702, and 705 systems. With all off-line equipment where a card reader is necessary, the 714 is used.

Except for the Charactron, to be discussed further below, and the camera device on the RCA-BIZMAC, non-mechanical printers are not important for use with most large scale systems, especially those discussed here. To be sure, many such devices have undergone some development as for example, the development of Atomic Instrument Company* which uses Teledeltos paper or that of General Electric Laboratory* which uses Ferromagnetography. However, these developments have not assumed a role of primary importance for use with large scale computing systems.

Electric typewriters have been used extensively for output of large systems but more recently have been on the decline, except for use in monitoring, in favor of line printers. Confining our discussion momentarily to on-line devices, the one in greatest use is the IBM 716 and 717 printers. Both print at 150 lines per minute and both designs are modified 407 Accounting Machine designs. The 716 has a control panel while the 717, in use with the 702, and 705, does not. The Bull Company makes a 150 line per minute printer which is available on 1103 and 1103A systems. A serious limitation of the Bull equipment is that only approximately 32 characters can be printed.

---

* See, for example, "Non-mechanical High-Speed Printers" by R. J. Rossheim, Proceedings of the Eastern Joint Computer Conference, March, 1953.

** Recently, RCA announced the availability of certain punched card equipments with the BIZMAC system.

But the equipment commanding the most attention (and highest rental fees) are those used off-line in transferring data at high speeds to and from magnetic tape. Off-line equipment transferring data from cards to printed page — the familiar accounting machine, from paper tape to cards, or from paper tape to printed page have been available in many forms for many years. The magnetic tape-driven equipments are a development of only the last few years.

The Eckhert-Mauchly Corporation, now part of Sperry-Rand, was the first to develop equipment to place information directly onto magnetic tape and directly remove that information. The Unityper, available since about 1951, allows direct keyboard-to-magnetic tape recording. The Unityper, still in use with Univac systems allows characters to be stored on tape in 120-character "blockettes" for subsequent read-in into the computer. The Uniprinter, also available when the first Univac was completed, is essentially an electric typewriter which prints information stored on magnetic tape at a printing rate of 10 characters per second.

One of the most serious faults of the Unityper is that items cannot be changed on a tape without re-recording the entire record. Also, automatic verification of information is not possible -- tapes are either read by the Uniprinter and checked by reading, or two tapes are independently prepared for subsequent machine chack. Sperry-Rand has under development a Tape Verifier which will appear this year. It will allow flexible, complete operation for original recording and tape verification.

Besides the Uniprinter and Unityper, Sperry-Rand has machines to transfer information from magnetic tapes to punched cards and vice-versa. The magnetic-tape-to-punched card converter takes information from Univac tapes to the conventional 80-column, 12-row cards at a rate of 120 cards per minute. The punched card-to-magnetic tape converter places information stored on the conventional cards and places it onto magnetic tape at the rate of 240 cards per minute. This machine is somewhat unusual in the sense that a suction mechanism picks cards from the hopper pile rather than the "picker-knife" mechanism usually seen. Equipment made and rented by International Business Machines are very similar in function and operating speeds. In addition, the IBM-774 or Tape Data Selector, allows an arbitrary selection of magnetic tape data for simultaneous output onto two or more devices such as card punches or accounting machines.

Magnetic tape controlled line printers are a most important new development. These machines with printing rates of 500 lines per second and upward are as expensive to buy or rent as many small magnetic drum computers and, in many cases, take up more space. Two line printers will be discussed here in some detail: the IBM-719 or 720, or 730 and the Remington Rand High Speed Printer. Another such printer will be available with RCA-BIZMAC systems.

The Remington Rand printer operates at 600 lines per minute, printing 120-character blockettes in 130 possible positions, with 51 different characters available in each position. Printing is accomplished by hammers which hit revolving type wheels at precise moments to select the appropriate character. Control is maintained by a number of means. A plugboard is available for the following: select characters from the blockette for selected placement in the 130 positions; multiple printing of certain character positions (10 duplicated, arbitrary, positions are available, the difference between 120 in the blockette and the 130 printing positions); multi-line printing of characters; line spacing; and zero suppression. Control of fast feed — skipping lines — is available

by means of a 7-channel paper tape loop which is used in conjunction with the first character (a non-printing character) stored in the blockette. A breakpoint switch, when set, will cause the machine to halt whenever the breakpoint symbol appears in the blockette. Fast-feed of the printer occurs at 20 inches per second. The printer has four pieces of equipment: the printer, a magnetic tape unit, a memory unit, and a power supply unit. The last two units require a supply of chilled water for cooling.

IBM makes three magnetic tape-driven high-speed line printers, all three very similar. The Type 719 operates at 1000 lines per minute with 60 printing positions, Type 720 operates at 500 lines per minute with 120 printing positions, and Type 730, 1000 lines per minute with 120 printing positions. In each case, printing of each character is accomplished by selection of a pattern of wires chosen from a 5 x 7 array. Fast feed is performed at about 50 inches per second for 4-5 inch skips on the 719 and 730, and at 25 inches per second on the 720. A paper tape loop in conjunction with the first character stored in the record control skips. No plugboard is available to control information; all such control is accomplished during the initial recording of the information on tape.

The IBM printers have not been in customers hands long enough to make a thorough comparison of the two printers. However, from the standpoint of system design, certain observations can be made. Printing quality on individual characters seems to be superior with the Remington-Rand machine. Although because of the type of printing this advantage comes as no surprise, two disadvantages of the Remington Rand type of printing appear: vertical registry of characters in their line position is not as good, and the number of carbon copies possible is smaller. The plugboard control available on the Remington Rand machine will save considerable computer time necessary for editing output and will not be a disadvantage as long as plugboards need not be changed too frequently. The breakpoint feature of the Remington Rand machine allows certain operations the IBM counterpart does not. A big advantage of the Types 719 and 730 is, of course, the very fast speed of 1000 lines per minute.

It may be of some interest to remark here that the four organizations ordering 1103A computers, Boeing, Lockheed, Ramo-Wooldridge, and Holloman Air Force Base, are obtaining somewhat modified version of the Remington Rand printer for data reduction operations. Type wheels have been changed to remove certain characters and allow, in their place, certain vertical bars and marking symbols. Also, the gears on carriage control have been changed to allow a small spacing of 10 lines per inch instead of the usual 6. This will allow printing an analog-type plot in the reduction of telemetered data to an accuracy of one part in 480 (or two plots each at one part in 240 accuracy) at a spacing of 10 marks per inch. Such a modification of a line printer was first done (to this writer's knowledge) at the Boeing Airplane Company in 1952 when an IBM 407 accounting machine was so modified.

Another interesting means of computer output involves the use of the cathode ray tube. Because "printing" here is non-mechanical, achieved speeds are much greater. One of the first such devices was the Numeriscope, delivered to the National Bureau of Standards in 1951 by Engineering Research Associates. Another early application of the cathode ray tube for output was that used with the Whirlwind I computer at MIT. Cathode ray tube output received considerable impetus when the RAND Corporation began using a tube and a camera to record information from their 701 computer in a military application. The general design has been embodied in an output system which IBM makes available for the 704 computer. Under computer control the beam can be directed to one